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10/715,594	11/19/2003	David Walter Flynn	550-491	6449

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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,594	FLYNN, DAVID WALTER	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The abstract of the disclosure is objected to because it is not clear what is the purpose of the reference to Figure 8 at the bottom of the abstract. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 4, 8, and 23 are objected to because of the following informalities:

Claim 4 recites the limitation "said busy signal" in line 2. There is insufficient antecedent basis for this limitation in the claim. Replacing the word "said" with "a" is suggested.

In claims 8 and 23, line 3, the word "to" appears to be missing before the phrase "said processing configuration".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 5, 8-10 12-17, 20, 23-25, and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al., US Patent No. 5,760,636 in view of Clark et al., US Patent No. 6,425,086.

Re claims 1 and 16 Noble discloses apparatus and a method for processing data, said apparatus an method comprising:

a processing circuit having a power supply configuration (column 3, lines 27-30, lines 48-52, Figure 1, 13, column 5, lines 13-17, lines 27-31, lines 60-64, Figure 2, steps 20-22) driven by a clock signal (column 3, lines 19-25, Figure 1, 10, 12), said processing circuit being operable:

(i) in a processing mode to perform data processing operations when said power supply configuration has a processing configuration and said clock signal is clocked (column 2, line 66 – column 3, line 11, column 4, lines 37-40, lines 43-46, column 8, lines 19-25, lines 41-50, Figure 4, steps 40-45); and

(ii) a holding mode (column 4, lines 27-29, Figure 2, Low Power mode); and

a power supply (column 3, lines 27-30) and a clock signal control circuit (Figure 1, 12) responsive to a target rate signal (column 4, lines 50-54, Figure 1, SLOW#) to modulate a target rate mode control signal (column 3, lines 53-57, Figure 1, SLOW_LOCK#) to switch said processing circuit between said processing mode and said holding mode (column 5, lines 50-53, lines 60-64, lines 31-42, Figure 2).

Re claims 1 and 16, Noble fails to disclose in a holding mode to hold state without performing processing operations when said power supply has a holding configuration and said clock is stopped, and a target rate signal indicative of a target rate of data processing operations to be performed by said processing circuit (to modulate a target rate mode control signal to switch said processing circuits between said processing mode and said holding mode – addressed above and added here for clarity) so as to achieve said target rate.

Clark teaches a dynamic power control for low power processors (column 1, lines 7-9), wherein based on the dynamic changes in the processing load of the processor, the operating frequency and voltage are adjusted in order to meet the desired computational task (target rate) using a control word indicative of the target processing (column 2, lines 20-25, column 4, lines 50-67, column 5, lines 18-28, lines 34-40, Fig.1 CONTROL WORD). In addition, Clark teaches entering sleep mode (where internal clocks are stopped) before adjusting the operating voltage supplied by the voltage regulator, as described above (column 5, line 55 – column 6, line 2). In Clark, the adjustment of the processor's operating clock frequency and voltage is dynamic, based on the processing load (column 2, lines 20-25). Thus, the power consumption is improved without compromising the computational performance (target rate) (column 2, lines 7-11).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and method for dynamically adjusting the operating clock and voltage of a processor (including stopping of the internal processor clocks in sleep mode) in order to achieve the desired computational

task using control signal indicative of the target processing, as suggested by Clark with the apparatus and method disclosed by Noble in order to implement in a holding mode to hold state without performing processing operations when said power supply has a holding configuration and said clock is stopped, and a target rate signal indicative of a target rate of data processing operations to be performed by said processing circuit to modulate a target rate mode control signal to switch said processing circuits between said processing mode and said holding mode so as to achieve said target rate. One of ordinary skill in the art would be motivated to do so in order to improve power consumption without compromising the target rate.

Re claims 2 and 17, Clark further teaches the apparatus and method, comprising one or more further circuits coupled to said processing circuit (column 4, lines 36-40 Fig. 2, 130).

Re claims 5 and 20, Noble further discloses the apparatus and method, wherein aid power supply and clock signal control circuit is responsive to apriority signal to override said target rate mode control signal to:

(i) switch said processing circuit from said holding mode to said processing mode independent of said target rate (column 7, lines 37-40, column 8, lines 29-35); and

(ii) to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate (column 7, lines 37-40, column 8, lines 29-35).

Re claims 8 and 23, Noble further discloses the apparatus and method, wherein said holding configuration corresponds to a power supply to said processing circuit having a potential difference lower than said potential difference corresponding to said processing configuration (column 4, lines 43-49).

Re claims 9 and 24, Noble further discloses the apparatus and method, as claimed in claims 8 and 23, wherein said processing circuit has a lower power consumption configuration when in said holding mode than when in said processing mode (column 1, lines 58-64, column 4, lines 27-29, lines 37-49).

Re claims 10 and 25, Noble further discloses the apparatus and method, as claimed in claims 8 and 23, wherein in said holding mode said potential difference of said power supply to said processing circuit is insufficient to allow said processing circuit to be clocked (column 6, lines 31-48, column8, lines 41-50).

Re claims 12 and 27, Noble further discloses the apparatus and method, wherein said processing circuit is a processor core (column 1, lines 7-10, Figure 1, 10).

Re claims 13 and 28, Noble further discloses the apparatus and method, as claimed in claims 2 and 17, wherein active high signaling is used from said processing circuit and said one or more further circuits (column4, line 64 – column 5, line 12).

Re claims 14 and 29, Noble further discloses the apparatus and method, comprising a clock generator operable to generate a clock source signal having a

fixed frequency which is selectively supplied to said processing circuit in dependence upon whether said processing circuit is in said processing mode or said holding mode (column 5, lines 53-59).

Re claims 15 and 30, Noble further discloses the apparatus and method, as claimed in claims 14 and 29, comprising a power supply generator, wherein when switching from said holding mode to said processing mode, said power supply generator sends a ready signal to said clock generator to indicate that said power supply configuration has reached said processing configuration such that said clock signal may be started (column 6, lines 31-48, Figure 2).

Claims 11 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al., US Patent No. 5,760,636 in view of Clark et al., US Patent No. 6,425,086, and further in view of Kusaka et al., US patent No. 4,823,309.

Re claims 11 and 26, Noble and Clark disclose the apparatus and method as per claims 1 and 16.

Noble and Clark fail to disclose one or more clamping circuits are provided between said processing circuit and said one or more further circuits.

Kusaka teaches a data processing circuit with an improved output circuit (column 1, lines 45-46) allowing the data processing circuit to interface with any kind of peripheral circuit by selecting its output state in the standby mode (column 1, lines 56-58) during which the clock signals applied to the processing system are blocked or discontinued, thus reducing the power consumption (column 1, lines 16-20). Kusaka further teaches a clamp circuit implementing the

above-mentioned functionality (column 3, line 49 – column 4, line 25, FIG. 3, FIG. 4). In Kusaka, the clamp circuit provides selectively a high impedance state and a clamped state in standby mode (column 1, lines 50-55). Thus, increased design flexibility and high performance are obtained depending on the type of peripheral attached to the data processing circuit (column 1, lines 36-41).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the clamp circuit used for interconnecting a data processing circuit and a peripheral device, as suggested by Kusaka with the apparatus and method disclosed by Noble and Clark in order to implement one or more clamping circuits are provided between said processing circuit and said one or more further circuits. One of ordinary skill in the art would be motivated to do so in order to increase the design flexibility and performance when interconnecting the processing circuit with the one or more further circuits.

Claims 3, 4, 6, 7, 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al., US Patent No. 5,760,636 in view of Clark et al., US Patent No. 6,425,086, and further in view of Maher et al., US Patent No. 6,088,807.

Re claims 3 and 18, Noble and Clark disclose the apparatus and method as per claims 1 and 16.

Noble and Clark fail to disclose said processing circuit is operable to generate a busy signal indicative of whether said processing circuit can be switched from said processing mode to said holding mode, said power supply and clock signal control circuit being responsive to said busy signal to override

said target rate mode control signal to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate.

Maher teaches a hardware control power management for microprocessor (column 1, lines 19-21) where determination is made whether to change the power mode without effecting the computer operation (column 3, lines 12-15, lines 20-22). Maher further teaches suspending the core processor clock after decision to enter reduced power mode (column 4, lines 46-55). In addition, Maher teaches a busy signal (column 4, lines 32-33, FIG. 3, BUSY) which prevents the core processor to switch into reduced power mode (even after proper assertion of suspend mode control signals) until the BUSY signal is cleared (i.e. no pending transactions are being executed) (column 5, lines 5-44, FIG. 4). Thus, the suspend control signal is overridden. In Maher, the apparatus and power control management method allow for enabling and disabling the microprocessor clock by utilizing a single control signal (column 2, lines 23-25). Thus, the power consumption is reduced without complicated circuitry (i.e. simplified and inexpensive design).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and method for power management utilizing a busy signal overriding the suspend control signal, as suggested by Maher with the apparatus and method disclosed by Noble and Clark in order to implement said processing circuit is operable to generate a busy signal indicative of whether said processing circuit can be switched from said processing mode to said holding mode, said power supply and clock signal control circuit being

responsive to said busy signal to override said target rate mode control signal to prevent a switch of said processing circuit from said processing mode to said holding mode independent of said target rate. One of ordinary skill in the art would be motivated to do so in order to achieve simple and inexpensive power management apparatus and method.

Re claims 4 and 19, Noble and Clark disclose the apparatus and method as per claims 2 and 17.

Noble and Clark fail to disclose said processing circuit is operable to assert said busy signal when a signal transfer is pending between said processing circuit and at least one of said one or more circuits.

Maher teaches a hardware control power management for microprocessor (column 1, lines 19-21) where determination is made whether to change the power mode without effecting the computer operation (column 3, lines 12-15, lines 20-22). Maher further teaches suspending the core processor clock after decision to enter reduced power mode (column 4, lines 46-55). In addition, Maher teaches a busy signal (column 4, lines 32-33, FIG. 3, BUSY) which prevents the core processor to switch into reduced power mode (even after proper assertion of suspend mode control signals) until the BUSY signal is cleared (i.e. no pending transactions are being executed by the co-processor) (column 5, lines 5-44, FIG. 4). Thus, the suspend control signal is overridden. In Maher, the apparatus and power control management method allow for enabling and disabling the microprocessor clock by utilizing a single control signal (column

2, lines 23-25). Thus, the power consumption is reduced without complicated circuitry (i.e. simplified and inexpensive design).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and method for power management utilizing a busy signal (active on pending transactions from the co-processor) overriding the suspend control signal, as suggested by Maher with the apparatus and method disclosed by Noble and Clark in order to implement said processing circuit is operable to assert said busy signal when a signal transfer is pending between said processing circuit and at least one of said one or more circuits. One of ordinary skill in the art would be motivated to do so in order to achieve simple and inexpensive power management apparatus and method.

Re claims 6 and 21, Noble and Clark disclose the apparatus and method as per claims 5 and 20.

Noble and Clark fail to disclose, wherein said priority signal is one of:

(i) an interrupt signal; and

(ii) a hardware real-time timer signal.

Maher teaches a hardware control power management for microprocessor (column 1, lines 19-21) where determination is made whether to change the power mode without effecting the computer operation (column 3, lines 12-15, lines 20-22). Maher further teaches suspending the core processor clock after decision to enter reduced power mode (column 4, lines 46-55). In addition, Maher teaches a busy signal (column 4, lines 32-33, FIG. 3, BUSY) which prevents the core processor to switch into reduced power mode (even after

proper assertion of suspend mode control signals) until the BUSY signal is cleared (i.e. no pending transactions are being executed by the co-processor) (column 5, lines 5-44, FIG. 4). In addition, Maher teaches the bus controller (i.e. logical circuit) receiving a plurality of income signals including the BUSY signal, the SUSP signal (indicative of power mode change), and two interrupt signals – INT and NMI (column 4, lines 26-26, FIG. 3) and generates a clock control signal (FIG. 3, F_SUSP) further used for switching between the suspended and normal operational mode. The interrupts received on the INT and NMI pins force the microprocessor to resume execution (column 6, lines 23-31) therefore preempting the suspend signal (column 6, lines 34) (i.e. higher priority signals). In Maher, the apparatus and power control management method allow for enabling and disabling the microprocessor clock by utilizing a single control signal (column 2, lines 23-25). Thus, the power consumption is reduced without complicated circuitry (i.e. simplified and inexpensive design).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and method for power management utilizing a combinatorial logic receiving the BUSY, SUSP, and INT or NMI priority signals and generating the clock control mode switching signal, as suggested by Maher with the with the apparatus and method disclosed by Noble and Clark in order to implement wherein said priority signal is one of: (i) an interrupt signal; and (ii) a hardware real-time timer signal. One of ordinary skill in the art would be motivated to do so in order to achieve simple and inexpensive power management apparatus and method.

Re claims 7 and 22, Noble and Clark disclose the apparatus and method as per claims 1 and 16.

Noble and Clark fail to disclose said target rate mode control signal, said busy signal and said priority signal are logically combined to generate a signal operable to switch said processing circuit between said processing mode and said holding mode.

Maher teaches a hardware control power management for microprocessor (column 1, lines 19-21) where determination is made whether to change the power mode without effecting the computer operation (column 3, lines 12-15, lines 20-22). Maher further teaches suspending the core processor clock after decision to enter reduced power mode (column 4, lines 46-55). In addition, Maher teaches a busy signal (column 4, lines 32-33, FIG. 3, BUSY) which prevents the core processor to switch into reduced power mode (even after proper assertion of suspend mode control signals) until the BUSY signal is cleared (i.e. no pending transactions are being executed by the co-processor) (column 5, lines 5-44, FIG. 4). In addition, Maher teaches the bus controller (i.e. logical circuit) receiving a plurality of income signals including the BUSY signal, the SUSP signal (indicative of power mode change), and two interrupt signals – INT and NMI (column 4, lines 26-26, FIG. 3) and generates a clock control signal (FIG. 3, F_SUSP) further used for switching between the suspended and normal operational mode. The interrupts received on the INT and NMI pins force the microprocessor to resume execution (column 6, lines 23-31) therefore preempting the suspend signal (column 6, lines 34) (i.e. higher priority signals).

Thus, the clock control signal is generated after logically combining the SUSP (i.e. target rate mode control signal), the BUSY signal, and both interrupt signals (i.e. priority signals). In Maher, the apparatus and power control management method allow for enabling and disabling the microprocessor clock by utilizing a single control signal (column 2, lines 23-25). Thus, the power consumption is reduced without complicated circuitry (i.e. simplified and inexpensive design).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and method for power management utilizing a combinatorial logic receiving the BUSY, SUSP, and INT or NMI signals and generating the clock control mode switching signal, as suggested by Maher with the with the apparatus and method disclosed by Noble and Clark in order to implement said target rate mode control signal, said busy signal and said priority signal are logically combined to generate a signal operable to switch said processing circuit between said processing mode and said holding mode. One of ordinary skill in the art would be motivated to do so in order to achieve simple and inexpensive power management apparatus and method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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